UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,112	07/03/2003	Lewis B. Aronson	15436.253.84	7667

22913 7590 05/23/2007

WORKMAN NYDEGGER
(F/K/A WORKMAN NYDEGGER & SEELEY)
60 EAST SOUTH TEMPLE
1000 EAGLE GATE TOWER
SALT LAKE CITY, UT 84111

EXAMINER	
LEUNG, CHRISTINA Y	
ART UNIT	**PAPER NUMBER**
2613	
MAIL DATE	**DELIVERY MODE**
05/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

5F

Office Action Summary	Application No.	Applicant(s)
	10/614,112	ARONSON ET AL.
	Examiner	Art Unit
	Christina Y. Leung	2613

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 03 April 2007.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6,8-12 and 14-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6,8-12 and 14-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 5, 6, 8, and 15-19** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites "said serial bus" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim because claim 1 on which claim 5 depends does not previously recite a serial bus. Examiner respectfully notes that claim 5 may be amended to depend on claim 4 instead. **Claims 6 and 8** depend on claim 5 and are therefore also indefinite for the same reasons as the parent claim.

Claim 15 recites "main controller IC" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim because although claim 1 on which claim 15 depends recites a "main controller," the claim does not previously recite a main controller integrated circuit.

Similarly, independent **claim 16** also recites "the main controller IC" in line 10 of the claim. There is insufficient antecedent basis for this limitation in the claim because although the claim recites "a main controller" in line 8, the claim does not previously recite a main controller integrated circuit. **Claims 17-19** depend on claim 16 and are therefore also indefinite for the same reasons as the parent claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1, 4-6, 8, 10-12, and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsuchiya et al. (US 5,040,242 A)** in view of **Shishikura et al. (US 6,488,416 B1)** and **Johansson (US 4,675,770 A)**.

Regarding **claims 1 and 14**, Tsuchiya et al. disclose an optical transceiver module (Figure 1), comprising

a plurality of components, the components including:

an optical transmitter (light emitting element 5); and

an optical receiver (light receiving element 7);

a power controller circuit (power supply circuit 41) electrically coupled to at least one of the plurality of components, where the power controller circuit is configured to perform power supply functions for the optical transceiver module and the power controller circuit includes multiple voltage regulators 12 and 13 configured and arranged to provide power to the components at two or more voltages (Figure 3 shows one embodiment of power supply circuit 41 in detail; column 7, lines 30-63); and

a main controller 20 electrically coupled to the optical transmitter 5, the optical receiver 7 and the power controller circuit 41 (column 5, lines 24-68; column 6, lines 1-59).

Examiner respectfully notes that although element 13 is labeled "DC-DC converter" by Tsuchiya et al., this element provides regulated voltage output (V2) and is therefore a voltage regulator. Tsuchiya et al. also disclose that element 12, which is more explicitly labeled "voltage regulator 12" may be implemented with a DC-DC converter (column 10, lines 10-13).

Further regarding claim 1, Tsuchiya et al. do not explicitly disclose that the components are contained within a housing, but it is well understood in the electronic and communications arts that optical and electrical elements may be encased in some type of housing.

Shishikura et al. in particular teach an optical module that is related to the one disclosed by Tsuchiya et al., including an optical transmitter, an optical receiver, and other electrical processing circuitry (Figure 18; column 9, lines 50-63) and further teach enclosing the module elements within a housing (see Figures 2 or 3, for example).

It would have been obvious to a person of ordinary skill in the art to specifically include a housing as suggested by Shishikura et al. in the system disclosed by Tsuchiya et al. simply in order to allow the module to be easily handled and protect the disclosed components from damage. One in the art would have been also motivated to provide a housing such as taught by Shishikura et al. in order to allow the module disclosed by Tsuchiya et al. to be securely placed within additional hardware as desired (see Shishikura et al., Figure 19, which shows how an optical module may be placed inside a computer, for example).

Further regarding claim 14 in particular, Tsuchiya et al. discloses that the power controller circuit is responsive to signals from the main controller

Further regarding both claims 1 and 14, Tsuchiya et al. do not explicitly disclose that the power control circuit 41 is an integrated circuit, but it is also well understood in the electronics

art that circuit elements may be integrated together. Johansson, for example, teaches a power controller comprising multiple voltage regulators in a single integrated circuit (see Figure and Abstract). Regarding claims 1 and 14, it would have been obvious to a person of ordinary skill in the art to integrate the power controller circuit elements and provide a power controller IC as taught by Johansson in the system described by Tsuchiya et al. in view of Shushikura et al. in order to manufacture the circuitry more compactly and efficiently.

Regarding **claims 4 and 5**, as well as claim 5 may be understood with respect to 35 U.S.C. 112 discussed above, Tsuchiya et al. disclose that the power controller circuit further includes a serial bus within the power controller circuit and that the multiple voltage regulators are electrically coupled to the serial bus (for example, Figure 3 shows a bus connecting regulators 12 and 13). Johansson, in the combination of Tsuchiya et al. in view of Shushikura et al. and Johansson, also further teaches a power controller IC including a serial bus within the power controller IC and that the multiple voltage regulators are electrically coupled to the serial bus (see Johansson, Figure).

Regarding **claim 6**, Tsuchiya et al. also disclose that the power controller circuit further comprises a serial interface electrically coupled to the serial bus (Figure 3 shows the bus connected to S1 output from processor 20).

Regarding **claim 8**, Tsuchiya et al. do not specifically disclose individually addressable voltage regulators, but Johansson further teaches voltage regulators that are individually addressable (column 1, lines 54-56). It would have been obvious to a person of ordinary skill in the art to use individually addressable voltage regulators as taught by Johansson in the system described by Tsuchiya et al. in view of Johansson in order to allow the system to operate the

multiple voltage regulators independently and thereby more effectively control the voltages output by the power controller.

Regarding **claim 10**, Tsuchiya et al. disclose that at least one of the voltage regulators is adjustable. Specifically, they disclose that threshold values may be adjusted in the regulator (column 8, lines 17-47). The voltage regulators taught by Johansson are also adjustable (Abstract).

Regarding **claim 11**, Tsuchiya et al. do not specifically disclose a temperature sensor as recited, but Johansson further teaches that the power controller includes temperature sensor 12 (column 2, lines 28-31). It would have been obvious to a person of ordinary skill in the art to include a temperature sensor as taught by Johansson in the system described by Tsuchiya et al. in view of Johansson in order to better protect the voltage regulators circuits from failures caused by excessive heat (Johansson, column 1, lines 27-51).

Regarding **claim 12**, Tsuchiya et al. disclose that the components further include a driver 4 electrically coupled to the optical transmitter 5 and a post-amplifier 6 electrically coupled to the optical receiver. They do not specifically disclose that the driver is a laser driver for a laser. However, various types of light emitting elements for optical communication are well known in the art, including lasers such as further taught by Shishikura et al. (column 6, lines 36-53). It would have been obvious to a person of ordinary skill in the art to specifically use a laser as taught by Shishikura et al. in the system described by Tsuchiya et al. in view of Shishikura et al. and Johansson as an engineering design choice of a way to effectively implement the light emitting element already disclosed by Tsuchiya et al. using a well known and widely available component.

Further regarding claim 12, Tsuchiya et al. do not specifically disclose that the driver circuit and the post-amplifier circuit are integrated circuits, but again, it is also well understood in the electronics art that circuit elements may be integrated together (as specifically taught by Johansson with respect to the power controller as already discussed above). Shishikura et al. also further teach that laser driver and amplifier elements in an optical transceiver may comprise integrated circuits (column 6, lines 50-54; column 7, lines 14-19). It would have been obvious to a person of ordinary skill in the art to separately integrate the driver circuit elements and the amplifier circuit elements in the system as suggested by Johansson and Shishikura et al. in the system described by Tsuchiya et al. in view of Shishikura et al. and Johansson in order to manufacture the circuitry groups more compactly and efficiently.

5. **Claims 2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsuchiya et al.** in view of **Shishikura et al.** and **Johansson** as applied to claim 1 above, and further in view of **Tse et al. (US 6,603,326 B1)**.

Regarding **claims 2 and 3**, Tsuchiya et al. in view of Shushikura et al. and Johansson describe a system as discussed above with regard to claim 1 including voltage regulators but they do not specifically disclose a low drop-out voltage regulator or a boost or buck regulator. However, various types of voltage regulators are generally well known in the art, and Tse et al. in particular teach low drop-out and buck regulator circuits for regulating voltage (column 1, lines 13-25; column 3, lines 66-67; column 4, lines 1-5).

Regarding claims 2 and 3, it would have been obvious to a person of ordinary skill in the art to use either a low drop-out voltage regulator or a boost or buck regulator as suggested by Tse et al. as the voltage regulator in the system described by Tsuchiya et al. in view of Shushikura et

al. and Johansson as an engineering design choice of a type of well known and widely available type of element to provide the disclosed voltage regulation function.

6. **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsuchiya et al.** in view of **Shushikura et al.** and **Johansson** as applied to claim 1 above, and further in view of **Lemon et al. (US 5,953,690 A)**.

Regarding **claim 9**, Tsuchiya et al. in view of Shushikura et al. and Johansson describe a system as discussed above with regard to claim 1. Tsuchiya et al. also disclose a light-receiving element 7 comprising a photodiode (column 11, line 18) and that at least one of the voltage regulators supplies voltage to receiver circuitry (Figure 1) but they do not specifically disclose an avalanche photodiode (APD) voltage supply.

However, various types of photodiodes are well known in the optical communications art. Lemon et al. in particular teach a system related to the one described by Tsuchiya et al. in view of Shushikura et al. and Johansson including an optical communications receiver (Figures 1, 2A, and 2B) and further teach an avalanche photodiode 501 having a controlled voltage supply (including APD voltage generator 524 and corresponding regulator 528).

It would have been obvious to a person of ordinary skill in the art to specifically use an avalanche photodiode as taught by Lemon et al. in the system described by Tsuchiya et al. in view of Shushikura et al. and Johansson as an engineering design choice of a way to implement the light receiving element already disclosed by Tsuchiya et al. using a well known and widely available component.

7. **Claims 1, 4-6, 8-12, and 14-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Anderson (US 5,929,982 A)** in view of **Shushikura et al.**, **Tsuchiya et al.**, and **Johansson**.

Regarding **claims 1, 15, and 16** Anderson discloses an optical transceiver module (Figure 8), comprising:

a plurality of components, the components including:

an optical transmitter (including laser 68); and

an optical receiver (including avalanche photodiode 80);

a plurality of addressable components (elements such as ROM 94 and RAM 96, for example);

a main controller (controller 90) electrically coupled to the optical transmitter and the optical receiver; and

an internal serial bus 92 connected to the main controller, optical transmitter, optical receiver, and an addressable component.

Further regarding claims 1, 15, and 16, Anderson does not explicitly disclose that the components are contained within a housing, but it is well understood in the electronic and communications arts that optical and electrical elements may be encased in some type of housing.

Shishikura et al. in particular teach an optical module that is related to the one disclosed by Tsuchiya et al., including an optical transmitter, an optical receiver, and other electrical processing circuitry (Figure 18; column 9, lines 50-63) and further teach enclosing the module elements within a housing (see Figures 2 or 3, for example).

Regarding claims 1, 15, and 16, it would have been obvious to a person of ordinary skill in the art to specifically include a housing as suggested by Shishikura et al. in the system disclosed by Anderson simply in order to allow the module to be easily handled and protect the disclosed components from damage. One in the art would have been also motivated to provide a housing such as taught by Shishikura et al. in order to allow the module disclosed by Anderson to be securely placed within additional hardware as desired (see Shishikura et al., Figure 19, which shows how an optical module may be placed inside a computer, for example).

Further regarding claims 1, 15, and 16, Anderson does not further specifically disclose a power controller integrated circuit. However, Tsuchiya et al. teach a system that is related to the one disclosed by Anderson including an optical transceiver module comprising an optical transmitter 5 and an optical receiver 7 (Figure 1). Tsuchiya et al. further teach a power controller circuit (power supply circuit 41) configured to perform power supply functions for the optical transceiver module and including multiple voltage regulators 12 and 13 configured and arranged to provide power to the components of the module at two or more voltages (Figure 3 shows one embodiment of power supply circuit 41 in detail; column 7, lines 30-63). It would have been obvious to a person of ordinary skill in the art to including a power controller circuit as taught by Tsuchiya et al. in the system described by Anderson and Shushikura et al. in order to effectively distribute and control the power to the various electronic and opto-electronic components of the transceiver module.

Further regarding claims 1, 15, and 16, Tsuchiya et al. do not explicitly further teach that the power control circuit 41 is an integrated circuit, but it is also well understood in the electronics art that circuit elements may be integrated together. Johansson, for example, teaches a

power controller comprising multiple voltage regulators in a single integrated circuit (see Figure and Abstract). Regarding claims 1, 15, and 16, it would have been obvious to a person of ordinary skill in the art to integrate the power controller circuit elements and provide a power controller IC as taught by Johansson in the system described by Anderon in view of Shushikura et al. and Tsuchiya et al. in order to manufacture the power controller circuitry already taught by Tsuchiya et al. more compactly and efficiently.

Regarding **claims 4 and 5**, as well as claim 5 may be understood with respect to 35 U.S.C. 112 discussed above, Tsuchiya et al., in the combination of Anderson in view of Shushikura et al., Tsuchiya et al., and Johansson, further teach that the power controller circuit further includes a serial bus within the power controller circuit and that the multiple voltage regulators are electrically coupled to the serial bus (for example, Figure 3 shows a bus connecting regulators 12 and 13). Johansson, in the combination of Anderson in view of Shushikura et al., Tsuchiya et al., and Johansson, also further teaches a power controller IC including a serial bus within the power controller IC and that the multiple voltage regulators are electrically coupled to the serial bus (see Johansson, Figure).

Regarding **claim 6**, Tsuchiya et al., in the combination of Anderson in view of Shushikura et al., Tsuchiya et al., and Johansson also teach that the power controller circuit further comprises a serial interface electrically coupled to the serial bus (Figure 3 shows the bus connected to S1 output from processor 20).

Regarding **claim 8**, Johansson, in the combination of Anderson in view of Shushikura et al., Tsuchiya et al., and Johansson, further teaches voltage regulators that are individually addressable (column 1, lines 54-56).

Regarding **claim 9**, the combination of Anderson in view of Shushikura et al., Tsuchiya et al., and Johansson, includes a voltage regulators supplying voltage to receiver circuitry as taught by Tsuchiya et al. (Figure 1). Anderson further discloses that the optical receiver comprises an avalanche photodiode 80.

Regarding **claim 10**, Tsuchiya et al., in the combination of Anderson in view of Shushikura et al., Tsuchiya et al., and Johansson, further teach that at least one of the voltage regulators is adjustable. Specifically, they disclose that threshold values may be adjusted in the regulator (column 8, lines 17-47). The voltage regulators taught by Johansson are also adjustable (Abstract).

Regarding **claim 11**, Johansson, in the combination of Anderson in view of Shushikura et al., Tsuchiya et al., and Johansson, further teaches a power controller IC including a temperature sensor 12 (column 2, lines 28-31). It would have been obvious to a person of ordinary skill in the art to include a temperature sensor as taught by Johansson in the system described by Anderson in view of Shushikura, Tsuchiya et al., and Johansson in order to better protect the voltage regulators circuits from failures caused by excessive heat (Johansson, column 1, lines 27-51).

Regarding **claim 12**, Anderson discloses that the components further include a laser driver 70 electrically coupled to the optical transmitter (laser 68) and a post-amplifier 86 electrically coupled to the optical receiver 80 (Figure 8).

Anderson does not specifically disclose that the driver circuit and the post-amplifier circuit are integrated circuits, but again, it is also well understood in the electronics art that circuit elements may be integrated together (as specifically taught by Johansson with respect to the power controller as already discussed above). Shishikura et al. also further teach that laser

driver and amplifier elements in an optical transceiver may comprise integrated circuits (column 6, lines 50-54; column 7, lines 14-19). It would have been obvious to a person of ordinary skill in the art to separately integrate the driver circuit elements and the amplifier circuit elements in the system as suggested by Johansson and Shishikura et al. in the system described by Anderson in view of Shushikura et al., Tsuchiya et al., and Johansson in order to manufacture the circuitry groups more compactly and efficiently.

Regarding **claim 14**, Tsuchiya et al., in the combination of Anderson in view of Shushikura et al., Tsuchiya et al., and Johansson, further teach that the power controller circuit is responsive to signals from a main controller (i.e., processor 20 as shown in Figure 1 of Tsuchiya et al.)

Regarding **claim 17**, Anderson discloses addressable components (specifically, ROM 94 and RAM 96) each comprising a memory. Anderson does not explicitly disclose that the addressable components 94 and 96 include a "serial interface" in those words, but does clearly disclose that the components are in communication with the bus 92. It is well understood in the art that a component attached to a bus would inherently include some interface simply to properly communicate information with the bus. It would have been obvious to a person of ordinary skill in the art to specifically include a serial interface element associated with each memory element simply in order to ensure that the components were in communication with the bus as already disclosed.

Regarding **claim 18**, Tsuchiya et al., in the combination of Anderson in view of Shushikura et al., Tsuchiya et al., and Johansson, further teach that the power controller circuit 41 is addressable by the main controller (processor 20; see Tsuchiya et al, Figure 1).

Regarding **claim 19**, Anderson discloses addressable components comprising a laser driver 70, a post-amplifier 86, an analog-to-digital converter 88, and an APD bias controller 84.

8. **Claims 2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Anderson** in view of **Shushikura et al.**, **Tsuchiya et al.**, and **Johansson** as applied to claim 1 above, and further in view of **Tse et al.**

Regarding **claims 2 and 3**, Anderson in view of Shushikura et al., Tsuchiya et al., and Johansson describe a system as discussed above with regard to claim 1 including voltage regulators but they do not specifically disclose a low drop-out voltage regulator or a boost or buck regulator. However, various types of voltage regulators are generally well known in the art, and Tse et al. in particular teach low drop-out and buck regulator circuits for regulating voltage (column 1, lines 13-25; column 3, lines 66-67; column 4, lines 1-5).

Regarding claims 2 and 3, it would have been obvious to a person of ordinary skill in the art to use either a low drop-out voltage regulator or a boost or buck regulator as suggested by Tse et al. as the voltage regulator in the system described by Anderson in view of Shushikura et al., Tsuchiya et al., and Johansson as an engineering design choice of a type of well known and widely available type of element to provide the disclosed voltage regulation function.

Response to Arguments

9. Applicant's arguments filed 03 April 2007 with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christina Y. Leung whose telephone number is 571-272-3023. The examiner can normally be reached on Monday to Friday, 7:30 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christina Y Leung
CHRISTINA LEUNG
PRIMARY EXAMINER